IN THE SPECIFICATION

Please amend the specification as follows:

Please amend paragraph [0021] as follows:

-- **[0021]** In even greater detail, level 3's TOQs are broken into as many sets 310 as there are child-links to bridge-bridge 200. Specifically, four child-links 221, 222, 223 and 224 are shown in parent-bridge 200, and each link has an associated TOQ set 310: 311, 312, 313 and 314 respectively, as well as their own transaction buffers 339. The child link 221 may include channels 219A-219N, which may be any number of channels that are utilized to communicate with the parent-bridge 232. It should also be appreciated that each of the other child-links may include various channels, as well. Further, within each TOQ set 310 there are as many TOQs 218 as there are grand-child links 285 for the associated child-link 220. For example, TOQ set 311, associated with child-link 221, and where such child-link 221 has four grand child links associated thereto: 286, 287, 288 and 289, is made up of four TOQs: 201, 202, 203 and 204. It should be noted that TOQ 203 is drawn in phantom form to show that it could represent multiple TOQs to assure that there were an equal amount of TOQs in set 311 as grand-child links associated with child-link 221. Each of the TOQ sets 310 contain a phantom TOQ for the same purpose. The remaining TOQ sets disclosed are as follows: TOQ set 312 contains TOQs 205, 206, 207 and 208; TOQ set 313 representing none or more TOQ sets 310, contains TOQs 209, 210, 211 and 212; and TOQ set 314 contains TOQs 213, 214, 215 and 216. Each of these TOQs 201-216 may include a TOQ identifier, such as TOQ identifiers 401-416, which are similar to the TOQ identifiers 441-456 discussed above. Other embodiments may use less than one TOQ per grand-child link 285 for the associated child-link 220, but a minimum of two such TOQs are needed to optimize transaction ordering. Further,

other multi-TOQ architectures use more or less number of links to more or less number of child-bridges or grandchild-links. --

Please amend paragraph [0024] as follows:

-- **[0024]** FIG. 4 shows the disclosed embodiment of FIG. 2 incorporated into a computer system 600. The computer system 600 includes CPU nodes 610, I/O nodes 630, and switch matrix 620. CPU nodes 610 include the four nodes 611, 612, 613 and 614. Each of the CPU nodes 611, 612, 613 and 614 includes one or more CPUs or processors. I/O nodes 630 include four I/O nodes 601, 602, 603 and 604. A switch fabric 620 is connected to CPU nodes 610 and to I/O nodes 630. The embodiment disclose in FIG. 2 is shown in FIG. 4 as I/O node 0. Like FIG. 2, I/O node 0 contains a parent-bridge 230. Parent –bridge 230 is attached via child –links 285 to child-bridges 260. The child-bridges 260, in turn, are connected via grand-child links 295 to buses 280~~230~~. Finally, buses 280~~230~~ are attached to I/O devices 290. It is contemplated, although not required, that some or all of the other I/O nodes would adopt a similar architecture shown in detail in I/O node 0. --